1/f Noise of NMOS and PMOS Transistors and their Implications to Design of Voltage Controlled Oscillators

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Abstract *Low frequency noise of NMOS and PMOS transistors in a 0.25-μm foundry CMOS process with a pure SiO_2 gate oxide layer is characterized for the entire range of MOSFET operation. Surprisingly, the measurement results showed that surface channel PMOS transistors have about an order of magnitude lower 1/f noise than NMOS transistors especially at V_{GS}-V_{TH} less than ~0.4V. The data were used to show that a VCO using all surface channel PMOS transistors can have ~14 dB lower close-in phase noise compared to that for a VCO using all surface channel NMOS transistors.*

I. Introduction

Low frequency noise in MOS transistors is critical in determining close-in phase noise of a voltage controlled oscillator. In order to understand the impact of low frequency noise to close-in phase noise of MOS voltage controlled oscillators, 1/f noise of NMOS and PMOS transistors in a 0.25-μm foundry CMOS process with a pure SiO_2 gate oxide layer has been characterized over the entire ranges for gate to source (V_{GS}) and drain to source (V_{DS}) voltages. The data are utilized to study close-in phase noise of VCO's using a time variant phase noise model [1]. The analyses show that 5.4-GHz PMOS VCO phase noise at a 50-kHz offset can be around 14 dB lower than NMOS VCO phase noise, which is indeed significant.

II. 1/f Noise of SCH CMOS Transistors

Fig. 1 shows normalized input referred 1/f noise (S_{VG}) for 0.25-μm channel length NMOS and PMOS transistors. A fortuitous unexpected result is that surface channel PMOS transistors have about an order of magnitude lower S_{VG} than NMOS transistors especially at V_{GS}-V_{TH} (V_{GT}) less than ~0.4V [2]. When V_{GT}'s are less than ~0.5 V, S_{VG}'s are independent of V_{GT} and in this regime, the 1/f noise modeling factors, K_F's for NMOS and PMOS transistors are 1.3×10^{-23} and 1.0×10^{-24} V^2F, respectively.

Output current noise PSD's versus I_{DS} plots for NMOS and PMOS transistors with a length and a width of 0.25 and 90 μm are shown in Fig. 2. Once again, PMOS noise is more than an order of magnitude lower than that for NMOS noise. I_{DS} has been changed by varying both V_{GT} and V_{DS}. It shows that S_{ID} is proportional to I_{DS}^{ξ} where ξ is 2 in

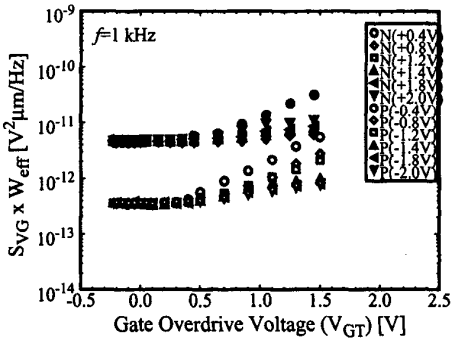

Fig. 1. Input referred noise PSD for an N- and a PMOS transistors at various drain-to-source voltages.(L=0.25 μm, W=90 μm) [2].

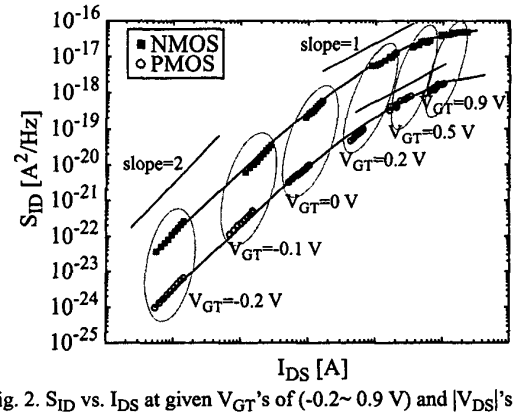

Fig. 2. S_{ID} vs. I_{DS} at given V_{GT}'s of (-0.2~ 0.9 V) and $|V_{DS}|$'s of (0.4-2.0 V).

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subthreshold and moderate inversion regions, but decreases as the degree of inversion increases. The plots show that I_{DS} changes due to varying V_{DS} and V_{GS} affect the current noise approximately in the same manner.

It has been generally believed and observed that PMOS transistors have 1~2 order(s) of magnitude lower 1/f noise than NMOS transistors because when an n^+-polysilicon gate layer is used for both NMOS and PMOS transistors, NMOS transistors have a surface channel (SCH) while PMOS transistors have a buried channel. As a result, the channel carriers in the former are closer to the Si/SiO_2 interface and have a higher probability of trapping and de-trapping by oxide traps, which are believed to be the major source of 1/f noise. In the 0.25-μm CMOS process, to deal with the short channel effects and high off current, p^+- poly gates are being used for PMOS transistors, while n^+-poly gates are used for NMOS transistors, thus making both types of transistors surface channel [3]. Because of this change, it has been expected that PMOS transistors would cease to have lower 1/f noise [4].

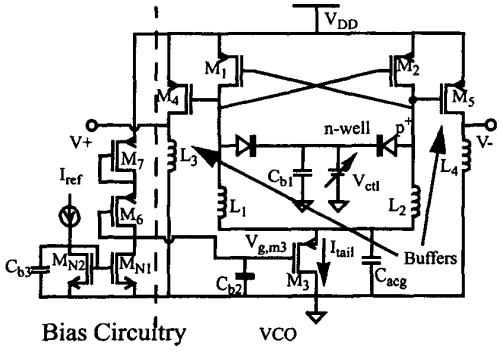

Fig. 3. A circuit schematic of the 5.4 GHz LC-VCO [7]

As discussed, the measurement results are in contradiction with this conventional wisdom. It turns out that around 6X of this ~10 X difference can be simply explained in terms of the differences in tunneling coefficients (λ in eqs. (1) and (2)) resulting from the differences in effective masses in SiO_2 and barrier heights of holes and electrons for tunneling into SiO_2 [2]. The

$$S_{VG} = \left(\frac{I_D}{g_m}\right)^2 \frac{q^4 \lambda N_T(E_{Fn})}{L^2 WkTf} \int_0^L \left(\frac{1 + Q_N \mu_N S}{C_{OX} + C_{DM} - \beta Q_N}\right)^2 dy \quad (1)$$

$$\lambda = h/\left[4\pi(2m^*\phi_B)^{1/2}\right] \quad (2)$$

barrier height for a hole (ϕ_{Bp}) is 4.7 eV while that for an electron (ϕ_{Bn}) is 3.1 eV [5]. Also, the effective mass of a hole in the oxide is 10~20 times heavier than that of an electron, i.e., $m_p^* = 5\sim10\ m_0$ and $m_n^*=0.5\ m_0$, where m_0 is the rest electron mass [5], [6].

III. Phase Noise of VCO Circuits

Before analyzing the impact of 1/f noise on phase noise, first, the 1/f noise data are used to compare the measured phase noise of 5.4 GHz differential VCO circuits shown Figs. 3 and 4, and that computed using the time variant phase noise model [1]. The VCO exclusively utilizes PMOS transistors for lower 1/f noise and potentially lower hot carrier induced white noise [7]. The VCO includes C_{acg} (20 pF) which AC grounds the source node of M_3 and keeps the drain to source voltage of M_3 essentially constant.

It has been suggested that the 1/f noise contributions from M_1 and M_2 to close-in phase noise can be neglected due to a reduction of 1/f noise in transistors with a switched gate which modifies the trapping and de-trapping processes for carriers [8],[9]. Because of this, only the 1/f noise of M_3 in the VCO core contributes to the phase noise. Furthermore, since the drain to source voltage of M_3 is constant, the effect of cyclic nature for V_{DS} bias for M_3 on 1/f noise can be neglected. This greatly simplifies the analyses and optimization of close-in phase noise of a VCO.

The phase noise of a VCO due to 1/f noise ($L(\Delta\omega)$) is expressed by [1]

$$L(\Delta\omega) \approx 10 \bullet \log\left[\frac{i^2_f c_0^2}{q_{max}^2 8(\Delta\omega)^2}\right] \quad (3)$$

where i^2_f is the 1/f current noise power spectral density at the DC operating point for the tail transistor (M_3), q_{max} is the maximum charge swing, $\Delta\omega$ is the offset frequency, and c_0 is the DC component or average of the impulse sensitivity function, $\Gamma(\omega_0\tau)$.

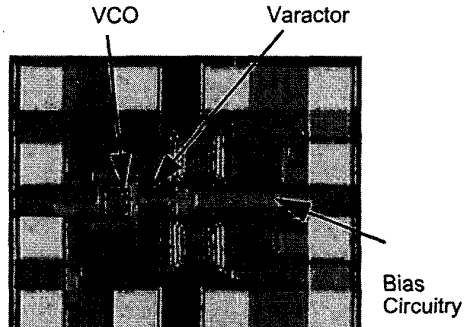

Fig. 4. A die photograph of 5.4 GHz LC-VCO [7]

The impulse sensitivity function, $\Gamma(\omega_0\tau)$ was simulated in a SPICE like tool by inserting a charge impulse (Δq) and measuring the resultant time shift (Δt) of the output wave form of the VCO circuit, which is related to the phase shift by $\Delta\phi=2\pi\Delta t/T$. The simulation circuit included inductor and varactor models based on measurements. It should be

noted that the phase shift ($\Delta\phi$) depends on the moment at which a charge pulse is inserted to a node of the VCO. The phase shift ($\Delta\phi$) becomes the maximum without an amplitude change (ΔV) when the charge impulse is inserted at a zero-crossing moment. On the other hand, ΔV becomes the maximum with $\Delta\phi=0$ when the impulse is inserted at the peak point of the output wave form. Fig. 5 illustrates the resulting amplitude change and phase shift when a charge impulse is inserted between a peak and a zero-crossing point. After a few periods, ΔV decays due to the automatic gain control function built into the VCO but $\Delta\phi$ persists indefinitely.

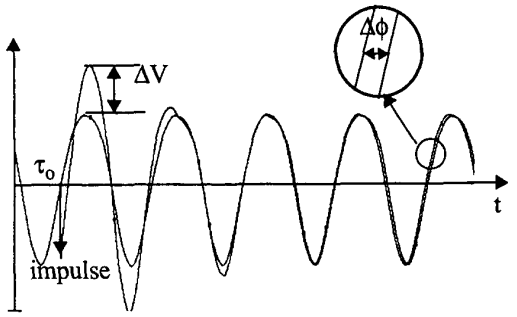

Fig. 5. Injection of an impulse (1 pC) at $t=\tau_0$ nsec into a node of a VCO and the resulting phase shift.

Fig. 6 shows the $\Gamma(\omega\tau_0)$ for transistors M_3 of the PMOS VCO as well as the wave form at drain node of M_2. C_0 which is the time averaged value for the ISF is 0.06.

A. 5.4 GHz PMOS LC VCO

Using the impulse sensitivity function ($\Gamma(\omega\tau_0)$) in Fig. 6 and 1/f noise data, the phase noise of PMOS LC VCO was predicted. The predicted phase noise at $\Delta\omega$=50 kHz was -87.5 dBc/Hz which was lower than the measured data in Fig.7 (-86 dBc/Hz) by 1.5 dB. Considering a typical variance of phase noise measurements, this ~1.5 dB difference is an excellent agreement, suggesting that the phase noise estimation procedure is working well. This also adds credence to the assertion that close-in phase noise contributions of M_1 and M_2 are small.

B. NMOS and PMOS LC VCO

To compare the phase noise performance of NMOS and PMOS voltage controlled oscillators, an NMOS VCO has been designed with the same process technology while using the same integrated inductors and keeping the current the same. A circuit schematic of the NMOS VCO is shown in Fig. 8. Once again, phase noise has been computed using the 1/f noise data. The circuit is exactly like the PMOS VCO except that all the PMOS transistors are replaced with NMOS transistors. The widths of NMOS transistors are around 1/3 of those of the transistors in the PMOS VCO.

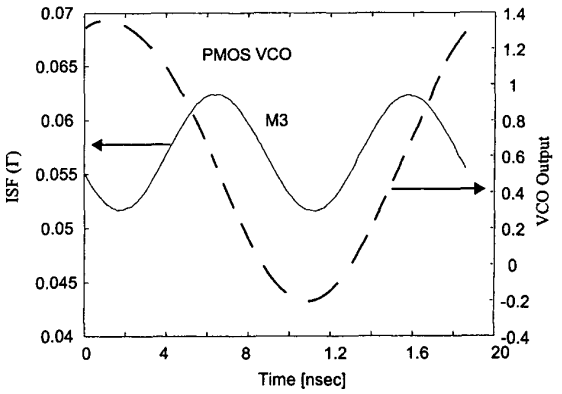

Fig. 6. $\Gamma(\omega\tau_0)$ for transistors M_3 of the PMOS VCO (c_0 = 0.06).

	Overall Phase Noise (dBc/Hz)
PMOS	-87.5
NMOS	-73.1

Table 1: Phase noise due to 1/f noise for PMOS and NMOS versions at Δf=50 kHz.

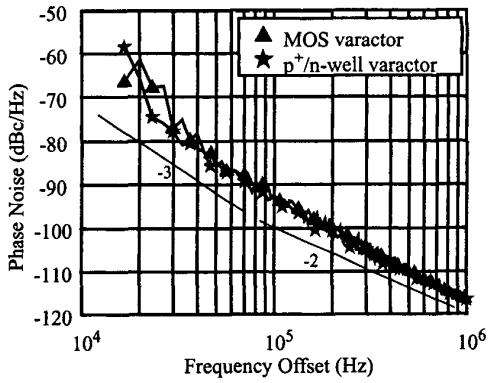

Fig.7. Measured phase noise of a 5.4-GHz VCO [1]

Fig. 9 shows the Γ plot for the NMOS VCO. C_0 is higher for the NMOS VCO due to a larger varactor [10]. The phase noise of PMOS VCO at a 50-kHz offset is 14 dB lower than that for the NMOS VCO, which is indeed significant. Of this difference, about 6 dB is due to the difference in c_0. The rest of differences is attributed to the differences in q_{max} for the VCO's, and more importantly to the differences in 1/f

noise. Table 1 summarizes the computed phase noise at an offset frequency of 50 kHz for both the NMOS and PMOS VCO's.

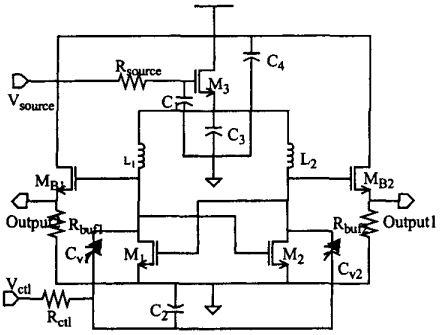

Fig. 8. NMOS LC-VCO circuit schematic.

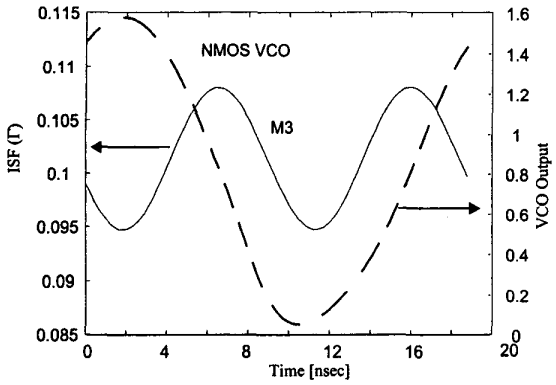

Fig. 9. $\Gamma(\omega\tau_0)$ for transistors M_3 of the NMOS VCO ($c_0 = 1.10$)

C. Tail transistor options

As discussed, the key to lower close-in phase noise of a VCO is lower 1/f noise of the tail transistor. There is a great deal of freedom in choosing a tail transistor beyond the choice between NMOS and PMOS transistors, since the tail transistor does not have to be a high speed device. For instance, since S_{id} is approximately proportional to $W^{-1}L^{-1}$, for a given current, the tail transistor width and length can be increased to lower 1/f noise at the cost of a larger layout area. Another is to operate the transistor in subthreshold and to forward bias the body to source junction by ~0.5 V, which has been shown to decrease 1/f noise by a factor of 10 [11]. Of course, using a bipolar tail transistor should significantly reduce close-in phase noise.

IV. Conclusions

In contradiction to the conventional wisdom, surface channel PMOS transistors can have lower 1/f noise than that for NMOS transistors. In the 0.25-μm foundry CMOS process with a pure SiO_2 gate oxide layer used for this study, surface channel PMOS transistors have about an order of magnitude lower 1/f noise than NMOS transistors especially at V_{GS}-V_{TH} less than ~0.4V. With the data, VCO's using entirely NMOS and entirely PMOS transistors have been compared. The phase noise of PMOS VCO at a 50-kHz offset is 14 dB lower than that for the NMOS VCO, which is significant. This indicates that VCO's implemented using surface channel PMOS transistors with a pure SiO_2 gate oxide layer can have superior phase noise than VCO's using surface channel NMOS transistors.

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